This Page Is Inserted by IFW Operations and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents will not correct images, please do not report the images to the Image Problem Mailbox.

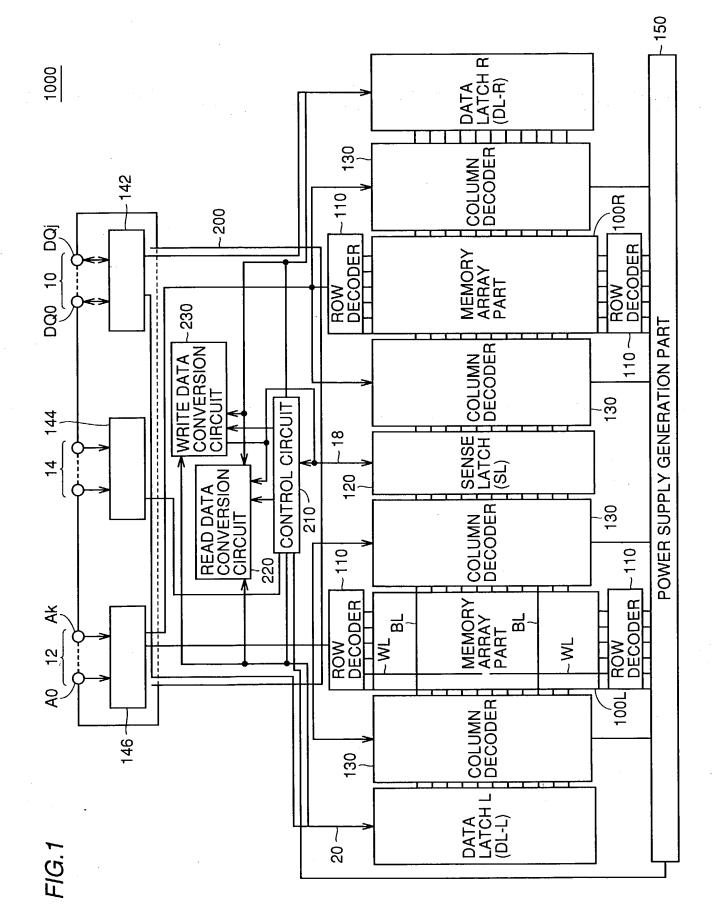




FIG.2

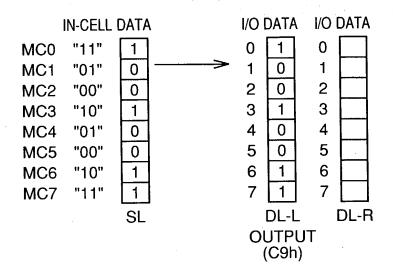


FIG.3

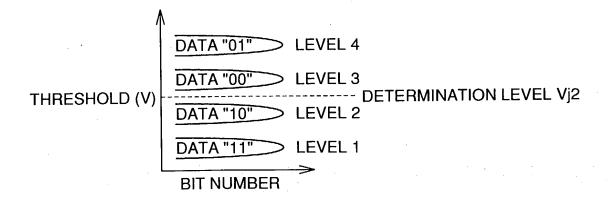




FIG.4

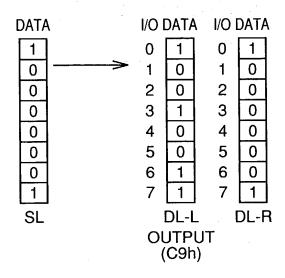


FIG.5

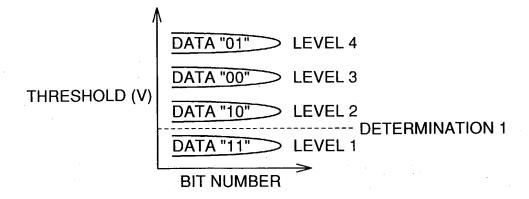




FIG.6

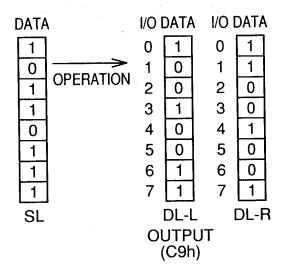
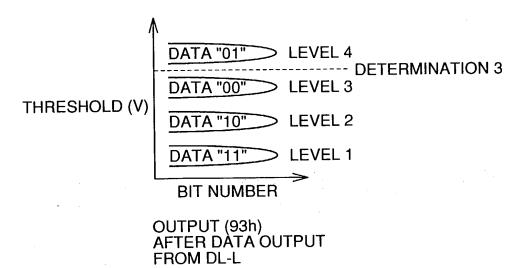
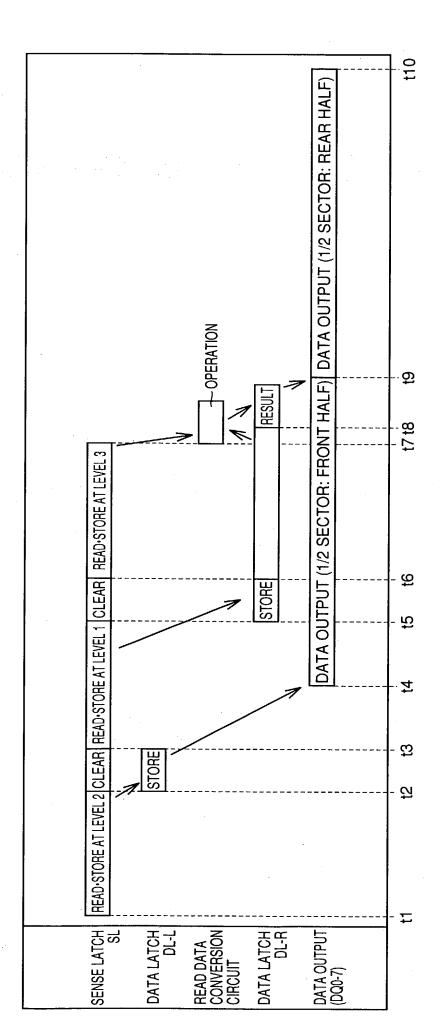


FIG.7







-/6.8



FIG.9

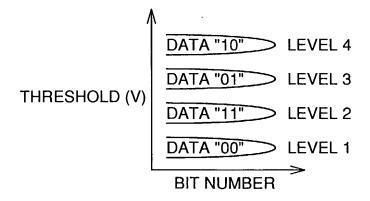
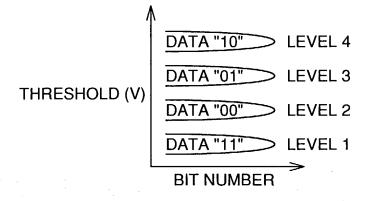
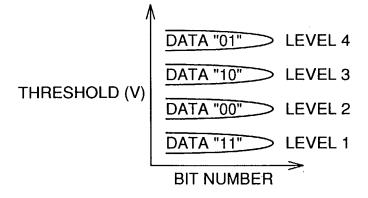
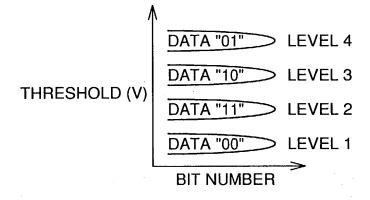


FIG.10

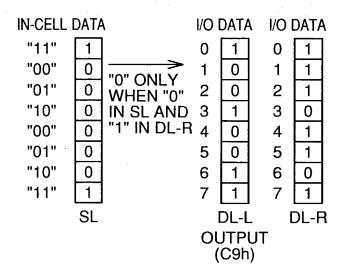


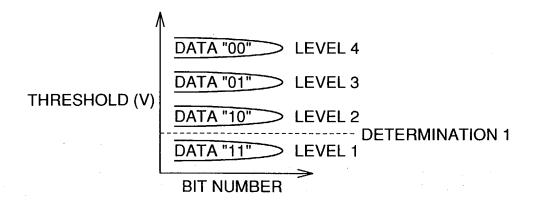














G,),:

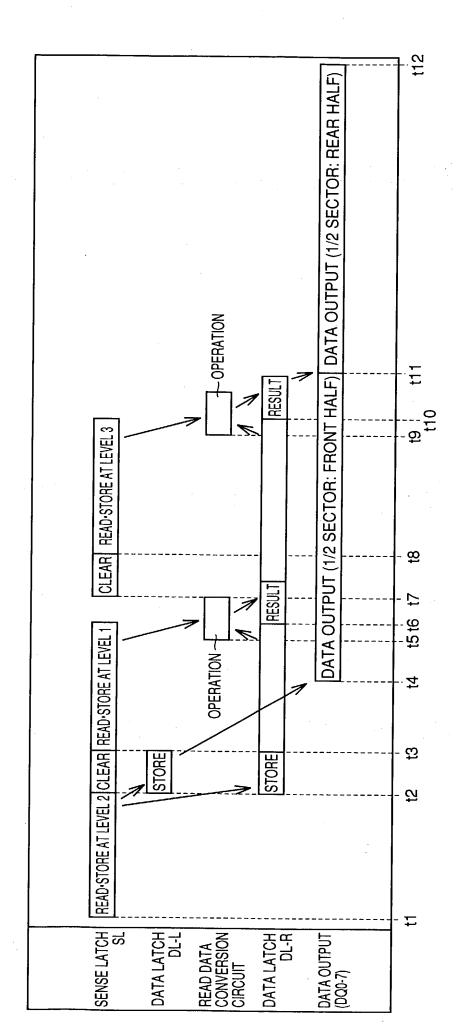


FIG. 15



FIG.16A FIG.16B

VI 120 WL 120 WL 120 BL1

SL BL1 BL1

BL2

FIG.17

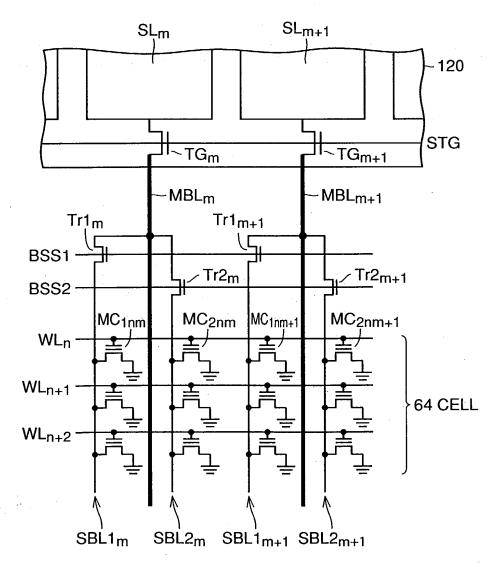




FIG.18

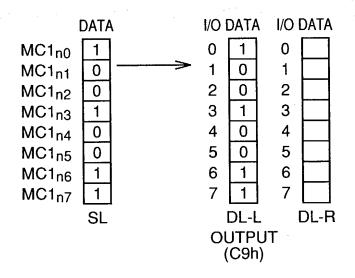


FIG.19

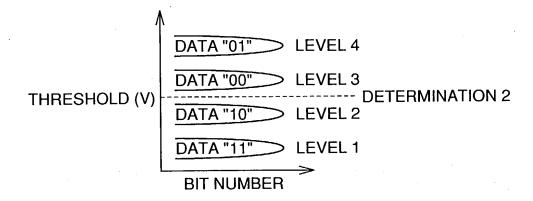




FIG.20

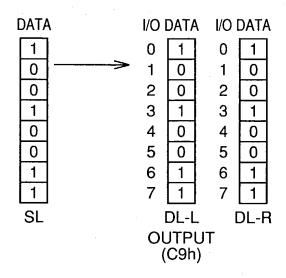


FIG.21

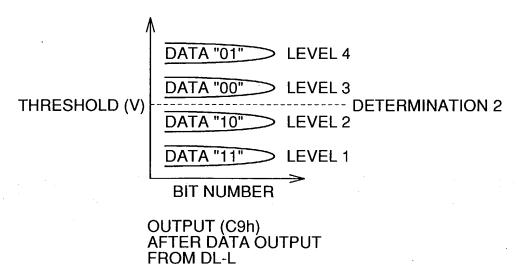
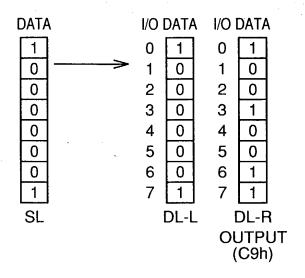
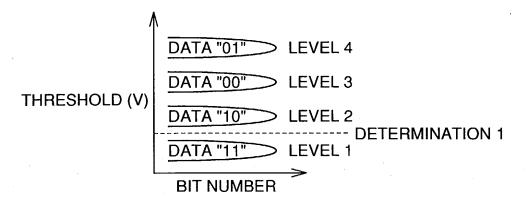




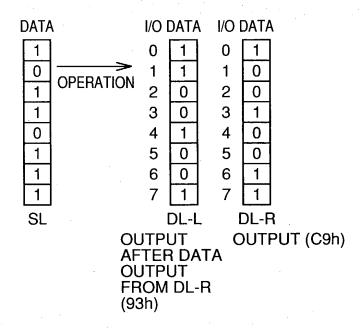
FIG.22





AUG 1 0 2004 TE

FIG.24



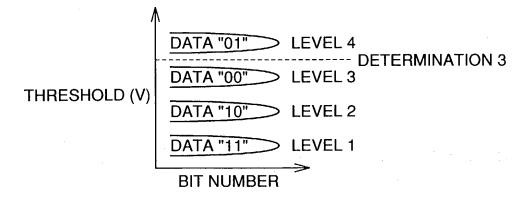




FIG.26

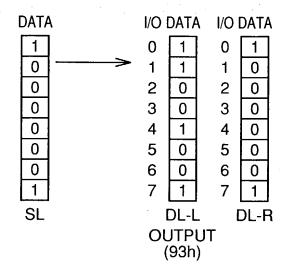


FIG.27

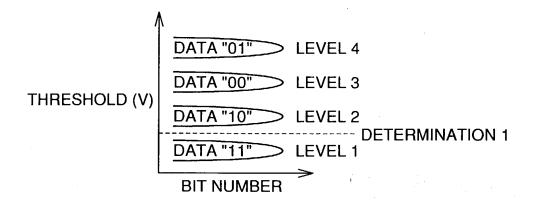
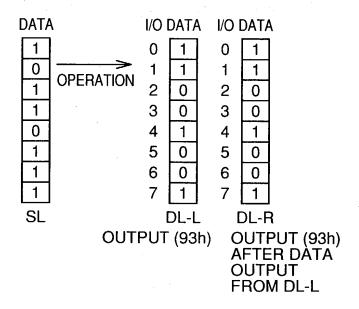
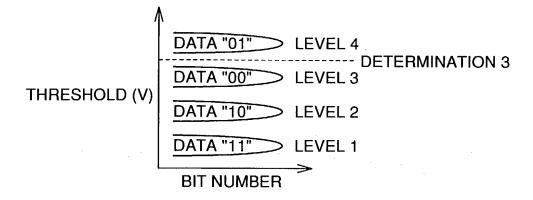




FIG.28







117 DATA OUTPUT 1 (1/4 SECTOR) DATA OUTPUT 2 (1/4 SECTOR) DATA OUTPUT 3 (1/4 SECTOR) DATA OUTPUT 4 (1/4 SECTOR) -OPERATION RESULT 115 CLEAR READ.STORE 2 AT LEVEL 3 CLEAR STORE †† 13 CLEAR READ·STORE 2 AT LEVEL 1 112 # OPERATION RESULT CLEAR READ-STORE 1 AT LEVEL 3 110 CLEAR STORE <u>8</u> 6 17 READ·STORE 1 AT LEVEL 1 φ. STORE CLEAR 5 CLEAR READ·STORE 2 AT LEVEL 2 ည STORE 口 READ-STORE 1 CAT LEVEL 2 SENSE LATCH SL READ DATA CONVERSION CIRCUIT DATA LATCH DL-R DATA OUTPUT (DQ0-7) DATA LATCH

-1G.3C



FIG.31

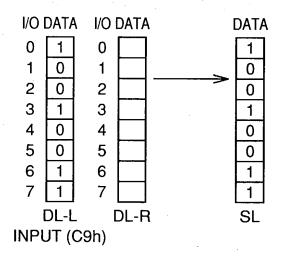


FIG.32

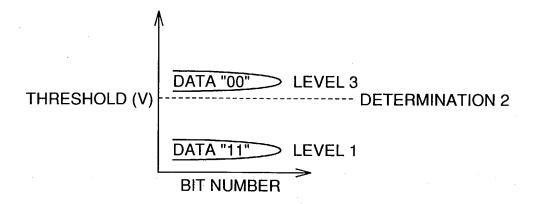




FIG.33

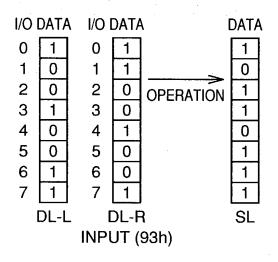


FIG.34

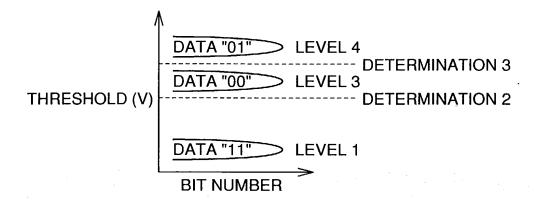




FIG.35

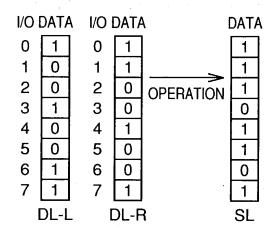
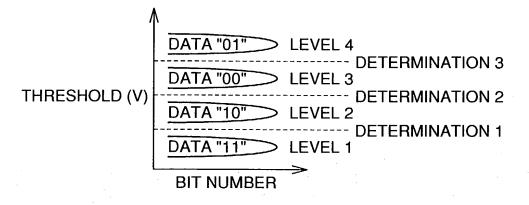
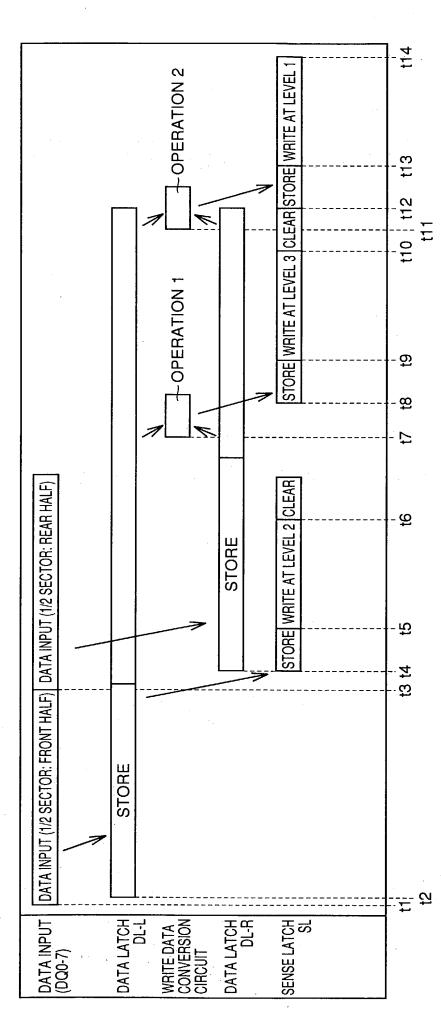


FIG.36







-16.3



FIG.38

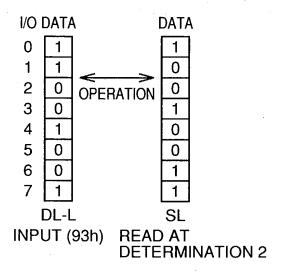


FIG.39

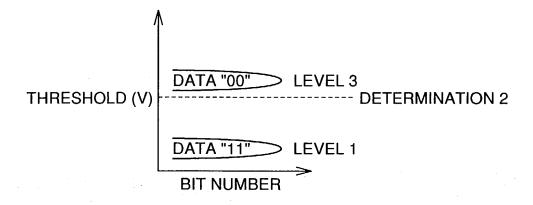
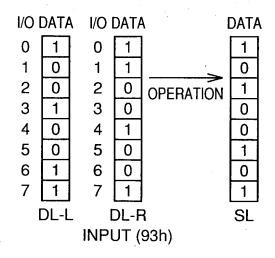
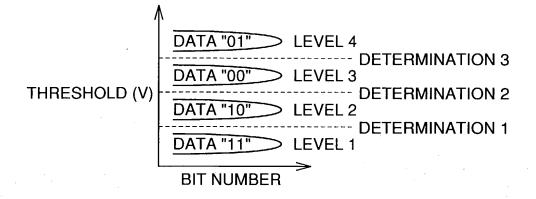


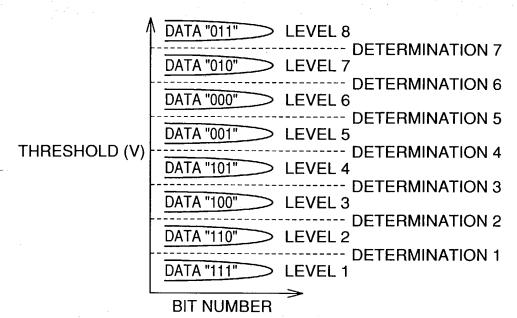


FIG.40





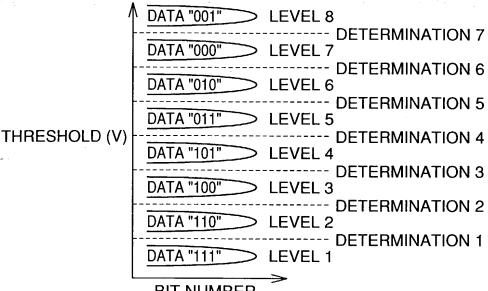




MOST SIGNIFICANT BIT DEFINED AT DETERMINATION 4 INTERMEDIATE BIT DEFINED AT DETERMINATION 2 & 6 LEAST SIGNIFICANT BIT DEFINED AT DETERMINATION 1, 3, 5 & 7

OK





BIT NUMBER

MOST SIGNIFICANT BIT DEFINED AT DETERMINATION 4 "0" & "1" AT LEVELS 3, 4, 5 & 6 AT DETERMINATION 2 & 6 NOT DEFINED LEAST SIGNIFICANT BIT DEFINED AT DETERMINATION 1, 3, 5 & 7

NG



FIG.44

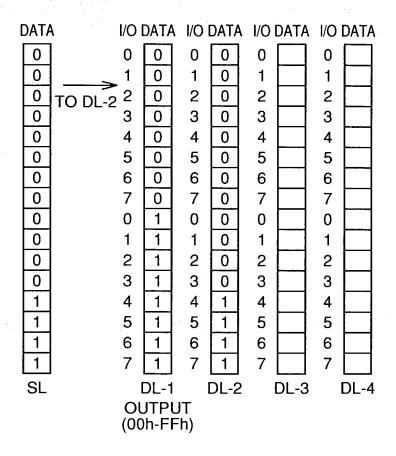
IN-CELL	DATA	I/O	DATA	1/0	DATA	1/0	DATA	I/O	DATA
MC0 "0111"	0	0	0	0		0		0	
MC1 "0110"	0 _	_ 1	0	1		1		1	
MC2 "0100"	0	2	0	2		2		2	
MC3 "0101"	0	3	0	3		3		3	
MC4 "0001"	0	4	0	4		4		4	
MC5 "0000"	0	5 ·	0	5		5		5	
MC6 "0010"	0	6	0	6		6		6	
MC7 "0011"	0	7	0	7		7		7	
MC8 "1011"	1	0	1	0		0		0	
MC9 "1010"	1	. 1	1	1		1		1	
MC10 "1000"	1	2	1	2	,	2		2	
MC11 "1001"	1	3	1	3		3		3	
MC12 "1101"	1	4	1	4		4		4	
MC13 "1100"	1	5	1	5		5		5	
MC14 "1110"	1	6	1	6		6		6	
MC15 "1111"	1	7	1	7		7		7	
	SL	1	DL-1	1	DL-2	[DL-3		 DL-4
			JTPU						
		(UU	h-FF	H)					

. .



/	DATA "0111"	LEVEL 16
	DATA "0110"	LEVEL 15
	DATA "0100"	LEVEL 14
•	DATA "0101"	LEVEL 13
	DATA "0001"	LEVEL 12
	DATA "0000"	LEVEL 11
	DATA "0010"	LEVEL 10
THRESHOLD (V)	DATA "0011"	LEVEL 9 DETERMINATION 8
·	DATA "1011"	
	DATA "1010"	LEVEL 7
	DATA "1000"	LEVEL 6
·	DATA "1001"	LEVEL 5
	DATA "1101"	LEVEL 4
·	DATA "1100"	LEVEL 3
	DATA "1110"	LEVEL 2
	DATA "1111"	LEVEL 1
_	BIT NUMBER	



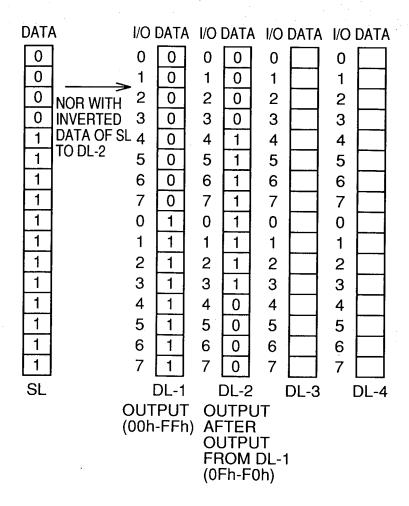




/	DATA "0111"	LEVEL 16	
	DATA "0110"	LEVEL 15	
	DATA "0100"	LEVEL 14	
	DATA "0101"	LEVEL 13	
	DATA "0001"	LEVEL 12	
	DATA "0000"	LEVEL 11	
•	DATA "0010"	LEVEL 10	
THRESHOLD (V)	DATA "0011"	LEVEL 9	
	DATA "1011"	LEVEL 8	
-	DATA "1010"	LEVEL 7	
	DATA "1000"	LEVEL 6	
	DATA "1001"		ETERMINIATION 4
	DATA "1101"		ETERMINATION 4
	DATA "1100"	LEVEL 3	
	DATA "1110"	LEVEL 2	
	DATA "1111"	LEVEL 1	
٠	BIT NUMBER		→



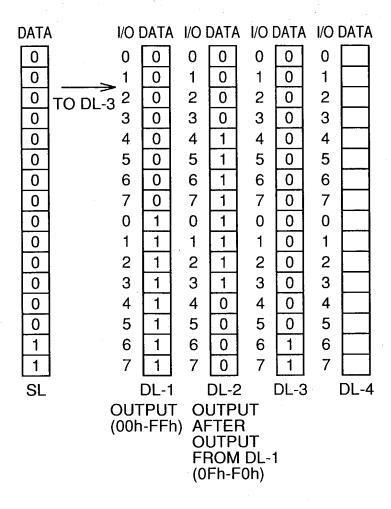
FIG.48





the second second	
1	DATA "0111" LEVEL 16
	DATA "0110" LEVEL 15
	DATA "0100" LEVEL 14
	DATA "0101" LEVEL 13
	DATA "0001" LEVEL 12
	DATA "0000" LEVEL 11
	DATA "0010" LEVEL 10
THRESHOLD (V)	DATA "0011" LEVEL 9
	DATA "1011" LEVEL 8
	DATA "1010" LEVEL 7
	DATA "1000" LEVEL 6
	DATA "1001" LEVEL 5
	DATA "1101" LEVEL 4
	DATA "1100" LEVEL 3
	DATA "1110" LEVEL 2
	DATA "1111" LEVEL 1
ı	BIT NUMBER







1	DATA "0111" LEVEL 16
	DATA "0110" LEVEL 15
·	DATA "0100" LEVEL 14
	DATA "0101" LEVEL 13
	DATA "0001" LEVEL 12
	DATA "0000" LEVEL 11
	DATA "0010" LEVEL 10
THRESHOLD (V)	DATA "0011" LEVEL 9
	DATA "1011" LEVEL 8
	DATA "1010" LEVEL 7
	DATA "1000" LEVEL 6
	DATA "1001" LEVEL 5
·	DATA "1101" LEVEL 4
	DATA "1100" LEVEL 3
	DATA "1110" LEVEL 2
	DATA "1111" LEVEL 1
	BIT NUMBER



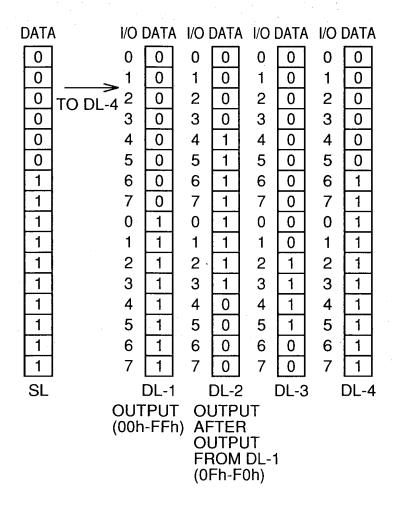
	FIG.52					
	DATA O O O O NOR WITH OINVERTED DATA OF TO DL-3 O O O O 1 1 1 1 1 SL	0 0 1 0 H 2 0 D 3 0 SL 4 0 5 0 6 0 7 0 0 1 1 1 2 1 3 1 4 1 5 1 6 1 7 1 OUTPUT	0 0 1 0 2 0 3 0 4 1 5 1 6 1 7 1 0 1 1 1 2 1 3 1 4 0 5 0 6 0 7 0 DL-2 OUTPL FROM	JT DL-1	I/O DATA 0	
·	SL .	OUTPUT	OUTPL AFTER OUTPL	JT JT DL-1	DL-4	



1	DATA "0111"	LEVEL 16
	DATA "0110"	LEVEL 15
	DATA "0100"	LEVEL 14
·	DATA "0101"	LEVEL 13
	DATA "0001"	LEVEL 12
	DATA "0000"	LEVEL 11
	DATA "0010"	LEVEL 10
HRESHOLD (V)	DATA "0011"	LEVEL 9
	DATA "1011"	LEVEL 8
	DATA "1010"	
	DATA "1000"	LEVEL 6
	DATA "1001"	LEVEL 5
	DATA "1101"	LEVEL 4
	DATA "1100"	LEVEL 3
	DATA "1110"	LEVEL 2
	DATA "1111"	LEVEL 1
	BIT NUMBER	>



FIG.54





1	DATA "0111"	LEVEL 16
	DATA "0110"	LEVEL 15
	DATA "0100"	LEVEL 14
	DATA "0101"	LEVEL 13
	DATA "0001"	LEVEL 12
	DATA "0000"	
	DATA "0010"	LEVEL 10
THRESHOLD (V)	DATA "0011"	LEVEL 9
	DATA "1011"	LEVEL 8
	DATA "1010"	LEVEL 7
	DATA "1000"	LEVEL 6
	DATA "1001"	LEVEL 5
	DATA "1101"	LEVEL 4
	DATA "1100"	LEVEL 3
	DATA "1110"	LEVEL 2
	DATA "1111"	LEVEL 1
	BIT NUMBER	



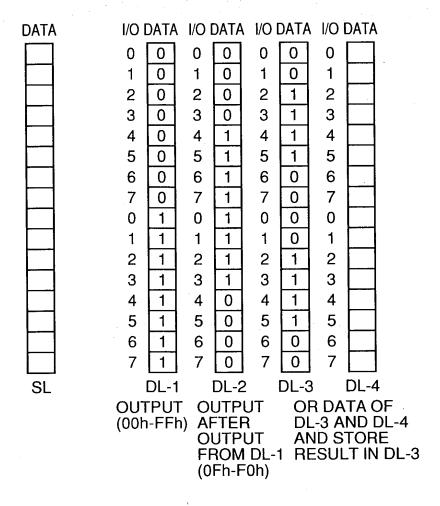
DATA	4	I/O	DATA	\	DATA	1/0	DATA	I/O	DATA
0		0	0	0	0	0	0	0	0
0		1	0	1	0	1	0	1	0
1	NOR	2	0	2	0	2	0	2	1
1	INVERTED	3	0	3	0	3	0	3	1
1	DATA OF SI	- 4	0	4	1	4	0	4	1
1	AND DATA OF DL-4	5	0	5	1	5	0	5	1
1	TO DL-4	6	0	6	1	6	0	6	0
1		7	0	7	1	7	0	7	0
1		0	1	0	1	0	0	0	0
1	·	1	1	1	1	1	0	1	0
1		2	1	2	1	2	1	2	0
1		3	1	3	1	3		3	0
1		4	1	4	0	4	1	4	0
1		5	1	5	0	5	1	5	0
1		6	1	6	0	6	0	6	0
1		7	1	7	0	7	0	7	0
SL			DL-1		DL-2		DL-3		DL-4
	OUTPUT OUTPUT (00h-FFh) AFTER OUTPUT FROM DL-1 (0Fh-F0h)								



^	DATA "0111" LEVEL 16
	DATA "0110" LEVEL 15 DETERMINATION 14
	DATA "0100" LEVEL 14
	DATA "0101" LEVEL 13
	DATA "0001" LEVEL 12
	DATA "0000" LEVEL 11
	DATA "0010" LEVEL 10
THRESHOLD (V)	DATA "0011" LEVEL 9
	DATA "1011" LEVEL 8
	DATA "1010" LEVEL 7
	DATA "1000" LEVEL 6
·	DATA "1001" LEVEL 5
	DATA "1101" LEVEL 4
	DATA "1100" LEVEL 3
	DATA "1110" LEVEL 2
	DATA "1111" LEVEL 1
	BIT NUMBER



FIG.58

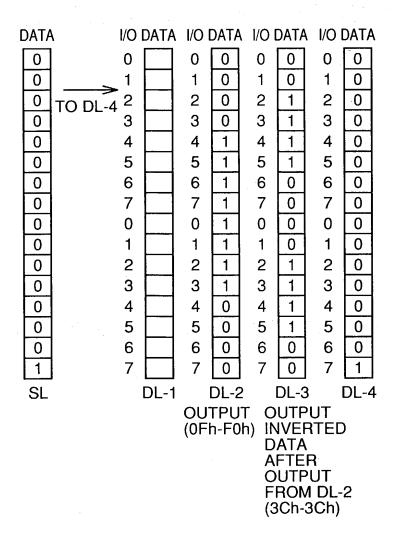




^	DATA "0111"	LEVEL 16
}	DATA "0110"	LEVEL 15
	DATA "0100"	
	DATA "0101"	LEVEL 13
	DATA "0001"	LEVEL 12
	DATA "0000"	LEVEL 11
	DATA "0010"	LEVEL 10
THRESHOLD (V)	DATA "0011"	LEVEL 9
	DATA "1011"	LEVEL 8
	DATA "1010"	LEVEL 7
·	DATA "1000"	LEVEL 6
	DATA "1001"	LEVEL 5
	DATA "1101"	LEVEL 4
	DATA "1100"	LEVEL 3
·	DATA "1110"	LEVEL 2
	DATA "1111"	LEVEL 1
· L	BIT NUMBER	



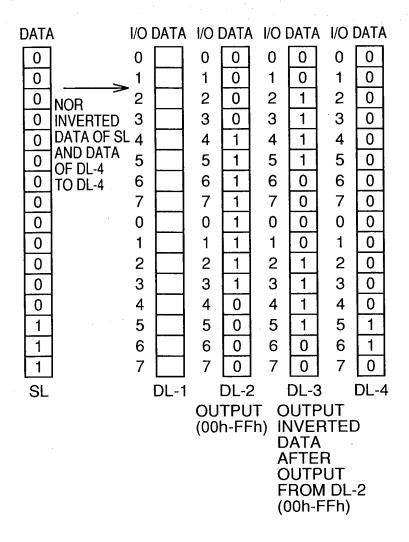
FIG.60





1	DATA "0111" LEVEL 16
	DATA "0110" LEVEL 15
	DATA "0100" LEVEL 14
	DATA "0101" LEVEL 13
	DATA "0001" LEVEL 12
	DATA "0000" LEVEL 11
	DATA "0010" LEVEL 10
THRESHOLD (V)	DATA "0011" LEVEL 9
	DATA "1011" LEVEL 8
	DATA "1010" LEVEL 7
	DATA "1000" LEVEL 6
	DATA "1001" LEVEL 5
	DATA "1101" LEVEL 4
	DATA "1100" LEVEL 3
	DATA "1110" LEVEL 2
	DATA "1111" LEVEL 1
L	BIT NUMBER







	•		
1	DATA "0111"	LEVEL 16	
	DATA "0110"	LEVEL 15	
	DATA "0100"	LEVEL 14	
	DATA "0101"	LEVEL 13	
	DATA "0001"	LEVEL 12	
	DATA "0000"	LEVEL 11	
	DATA "0010"	LEVEL 10	
THRESHOLD (V)	DATA "0011"	LEVEL 9	
	DATA "1011"	LEVEL 8	
	DATA "1010"	LEVEL 7	
	DATA "1000"	LEVEL 6	
	DATA "1001"	LEVEL 5	
·	DATA "1101"		
	DATA "1100"	LEVEL 3	DETERMINATION 3
	DATA "1110"	LEVEL 2	
	DATA "1111"	LEVEL 1	
	BIT NUMBER		→



DATA	I/O	DATA	I/O	DATA	1/0	DATA	I/O	DATA	
0	0	0	0	0	0	0	0	0	
0	_ 1	0	1	0	1	0	1	0	
TO DL-	1 2	0	2	0	2	1	2	0	
0	' 3		3		3	1	3	0	
0	4	0	4	1	4	1	4	0	
0	5	0	5	1	5	1	5	0	
0	6	0	6	1	6	0	6	0	
0	7	0	7	1	7		7		
0	0 1	0	0	1	0	0	0	0	
0		0	1	1	1	0	1.	0	
	2		2 3	$\frac{1}{1}$	2 3	1	2	0	
	4	$\frac{1}{1}$	4	\vdash	3 4	1	4	0	
1	5	$\frac{1}{1}$	5	0	5	1	5	1	
	6	1	6	0	6	0	6	1	
1	7	1	7	0	7	6	7	 	
SL	-	DL-1		ىت DL-2		DL-3		DL-4	
OL.	•	<i>D</i> L 1		TPU		UTP		DLT	
	(0Fh-F0h) INVERTED								
	DATA								
	AFTER OUTPUT								
	FROM DL-2								
					(3	Ch-3	Ch)		



/	DATA "0111"	LEVEL 16
	DATA "0110"	LEVEL 15
·	DATA "0100"	LEVEL 14
	DATA "0101"	LEVEL 13
	DATA "0001"	LEVEL 12
	DATA "0000"	LEVEL 11
	DATA "0010"	LEVEL 10
THRESHOLD (V)	DATA "0011"	LEVEL 9
	DATA "1011"	LEVEL 8
·	DATA "1010"	LEVEL 7
	DATA "1000"	
	DATA "1001"	LEVEL 5
	DATA "1101"	LEVEL 4
	DATA "1100"	LEVEL 3
	DATA "1110"	LEVEL 2
i s	DATA "1111"	LEVEL 1
	BIT NUMBER	



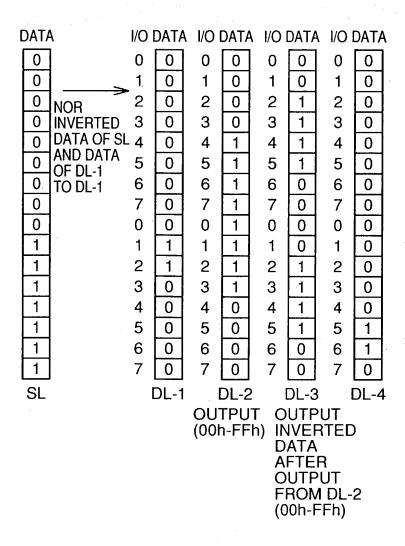




FIG.67	
1	DATA "0111" LEVEL 16
	DATA "0110" LEVEL 15
,	DATA "0100" LEVEL 14
	DATA "0101" LEVEL 13
- ·	DATA "0001" LEVEL 12
	DATA "0000" LEVEL 11
·	DATA "0010" LEVEL 10
THRESHOLD (V)	DATA "0011" LEVEL 9
	DATA "1011" LEVEL 8
	DATA "1010" LEVEL 7
	DATA "1000" LEVEL 6
	DATA "1001" LEVEL 5
·	DATA "1101" LEVEL 4
·	DATA "1100" LEVEL 3
	DATA "1110" LEVEL 2
	DATA "1111" LEVEL 1
L	BIT NUMBER

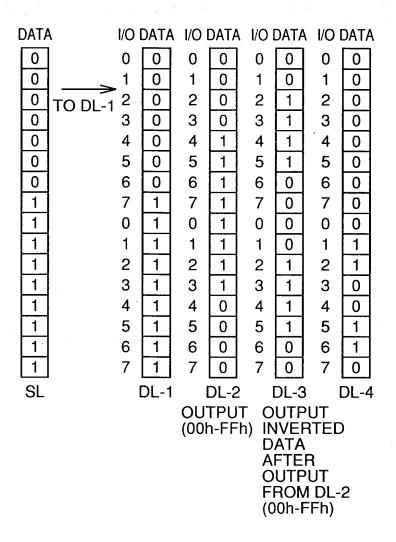


					[DL-1	ATA ANE		
DATA	1/0	DATA	I/O	DATA		DATA		DATA	١
DATA	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	OATA O O O O O O O O O O O O O O O O O	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 OU OU OU OU OU OU OU OU OU OU OU OU OU	DATA 0 0 0 1 1 1 1 1 0 0 DL-2 TPU	1/O 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7 OINDAO	0 0 1 1 1 0 0 0 0 1 1 1 1 0 0 UTP IVEF ATA FTEI UTP	1/O 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 0 0 0 0 0 0 1 1 0 0 1	
						Ch-		_	

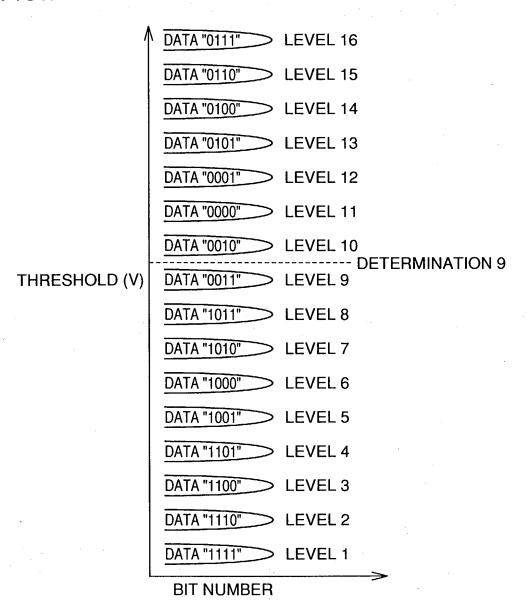


./	DATA "0111" LEVEL 16
	DATA "0110" LEVEL 15
	DATA "0100" LEVEL 14
	DATA "0101" LEVEL 13
	DATA "0001" LEVEL 12
	DATA "0000" LEVEL 11
	DATA "0010" LEVEL 10
THRESHOLD (V)	DATA "0011" LEVEL 9
	DATA "1011" LEVEL 8
·	DATA "1010" LEVEL 7
	DATA "1000" LEVEL 6
	DATA "1001" LEVEL 5
	DATA "1101" LEVEL 4
	DATA "1100" LEVEL 3
	DATA "1110" LEVEL 2
	DATA "1111" LEVEL 1
l.	BIT NUMBER











DATA	1	I/O	DATA	i/O I	DATA	I/O	DATA	I/O	DATA
0		0	0	0	0	0	0	0	0
0		1	0	1	0	1	0	1	0
0	NOR	2	0	2	0	2	1	2	0
0	INVERTED	3	0	3	0	3	1	3	0
0	DATA OF SI AND DATA	•	0	4	1	4	1	4	0
1	OF DL-1	5	1	5	1	5	1	5	0
1	TO DL-1	6	1	6	1	6	0	6	0
1		7	0	7	1	7	0	7	0
1		0	0	0	1	0	0	0	0
1		1	0	1	1	1	0	1	1
1		2	0	2	1	2	1	2	1
1		3	0	3 ,	1	3	1	3	0
1		4	0	4	0	4	1	4	0
1		5	0	- 5	0	5	1	5	1
1		6	0	6	0	6	0	6	1
1		7	0	7	0	7	0	7	0
SL			DL-1	1	DL-2		DL-3		DL-4
					TPU		UTP		
		(00h-FFh) INVERTED							
		DATA AFTER							
		OUTPUT							
							ROM		2
						(0)0h-F	· - h)	

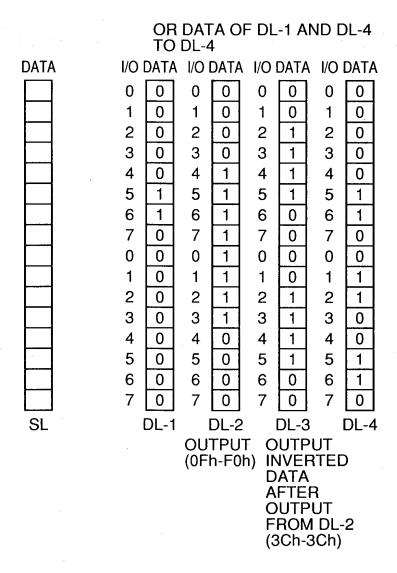
. . . !



	DATA "0111" LEVEL 16
	DATA "0110" LEVEL 15
	DATA "0100" LEVEL 14
	DATA "0101" LEVEL 13
	DATA "0001" LEVEL 12
	DATA "0000" LEVEL 11
	DATA "0010" LEVEL 10
THRESHOLD (V)	DATA "0011" LEVEL 9
	DATA "1011" LEVEL 8
· -	DATA "1010" LEVEL 7
	DATA "1000" LEVEL 6
	DATA "1001" LEVEL 5
	DATA "1101" LEVEL 4
	DATA "1100" LEVEL 3
	DATA "1110" LEVEL 2
	DATA "1111" LEVEL 1
·. .	BIT NUMBER



FIG.74





1	DATA "0111"	LEVEL 16
	DATA "0110"	LEVEL 15
	DATA "0100"	LEVEL 14
	DATA "0101"	LEVEL 13
·	DATA "0001"	
	DATA "0000"	LEVEL 11
	DATA "0010"	LEVEL 10
THRESHOLD (V)	DATA "0011"	LEVEL 9
	DATA "1011"	LEVEL 8
	DATA "1010"	LEVEL 7
	DATA "1000"	LEVEL 6
	DATA "1001"	LEVEL 5
	DATA "1101"	LEVEL 4
	DATA "1100"	LEVEL 3
	DATA "1110"	LEVEL 2
	DATA "1111"	LEVEL 1
L	BIT NUMBER	



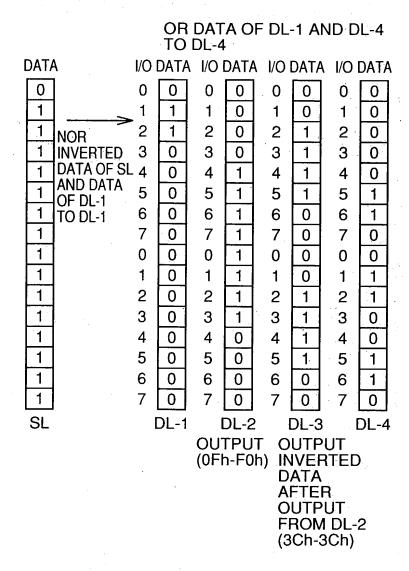
FIG.76

DATA	I/O	DATA	I/O I	DATA	1/0	DATA	1/0	DATA
0	0	0	0	0	0	0	0	0
	1	0	1	0	1	0	1	0
O TO DL-1		0	2	0	2	1	2	0
1	3	1	3	0	3	1	3	0
11	4		4	1	4	1	4	0
1	5		5	1	5	1	5	
1	6		6	1	6	0	6	1
1	7		7	1	7	0	7	0
1	0		0	1	0	0	0	0
1	1	1	1	1	1	0	1	1
1	2	1	2	1	2	1	2	1
1	3	1	3	1	3	1	3	0
1	4	1	4	0	4	1	4	0
1	5	1	5	0	5	1	5	1
1	6	1	6	0	6	0	6	1
1	7	1	7	0	7	0	7	0
SL		DL-1	1	DL-2		DL-3	}	DL-4
	OUTPUT OUTPUT (00h-FFh) INVERTED DATA)
	AFTER OUTPUT							
						ROM	1 DL-	2
					(0)0h-F	-Fh)	



•	
/	DATA "0111" LEVEL 16
	DATA "0110" LEVEL 15
	DATA "0100" LEVEL 14
	DATA "0101" LEVEL 13
	DATA "0001" LEVEL 12
	DATA "0000" LEVEL 11
	DATA "0010" LEVEL 10
THRESHOLD (V)	DATA "0011" LEVEL 9
	DATA "1011" LEVEL 8
	DATA "1010" LEVEL 7
	DATA "1000" LEVEL 6
	DATA "1001" LEVEL 5
	DATA "1101" LEVEL 4
	DATA "1100" LEVEL 3
	DATA "1110" LEVEL 2
	DATA "1111" LEVEL 1
l	BIT NUMBER

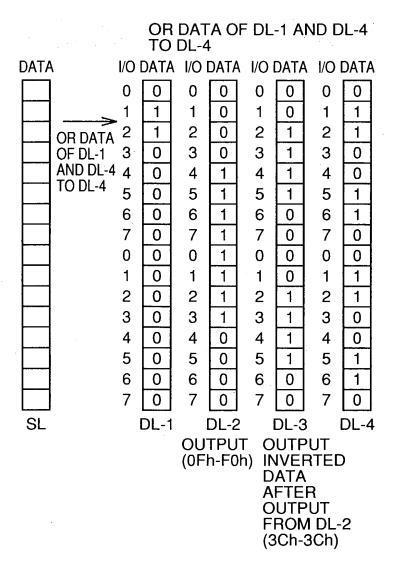






/	DATA "0111" LEVEL 16
	DATA "0110" DETERMINATION 15
	DATA "0100" LEVEL 14
	DATA "0101" LEVEL 13
	DATA "0001" LEVEL 12
	DATA "0000" LEVEL 11
	DATA "0010" LEVEL 10
THRESHOLD (V)	DATA "0011" LEVEL 9
	DATA "1011" LEVEL 8
	DATA "1010" LEVEL 7
:	DATA "1000" LEVEL 6
	DATA "1001" LEVEL 5
	DATA "1101" LEVEL 4
	DATA "1100" LEVEL 3
	DATA "1110" LEVEL 2
	DATA "1111" LEVEL 1
. [BIT NUMBER







1	DATA "0111" LEVEL 16
	DATA "0110" LEVEL 15
	DATA "0100" LEVEL 14
	DATA "0101" LEVEL 13
	DATA "0001" LEVEL 12
	DATA "0000" LEVEL 11
	DATA "0010" LEVEL 10
THRESHOLD (V)	DATA "0011" LEVEL 9
	DATA "1011" LEVEL 8
	DATA "1010" LEVEL 7
	DATA "1000" LEVEL 6
	DATA "1001" LEVEL 5
	DATA "1101" LEVEL 4
	DATA "1100" LEVEL 3
,	DATA "1110" LEVEL 2
	DATA "1111" LEVEL 1
; · · · · · · · · · · · · · · · · · · ·	BIT NUMBER



FIG.82

I/O	DATA	I/O	DATA	I/O	DATA	I/O	DATA		DATA
0	0	0		0		0			0
1	0	1		1		1		_	0
2	0	2		2		2		FROM	0
3	0	3		3		2 3		DL-1	0
4	0	4		4		4			0
5	0	5		5		5			0
6	0	6		6		6			0
7	0	7		7		7			0
0	1	0		0		0			1
1	1	1		1		1			1
2 3	1	2		2		2			1
3	1	3		3		3			1
4	1	4		4 5		4			1
5	1	5		5		5			1
6	1	6		6		6			1
7	1	7		7		7			1
-	DL-1		DL-2	į	DL-3		DL-4	•	SL



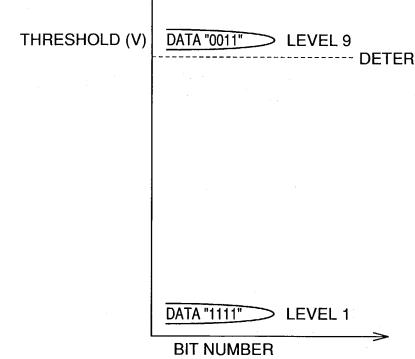




FIG.84

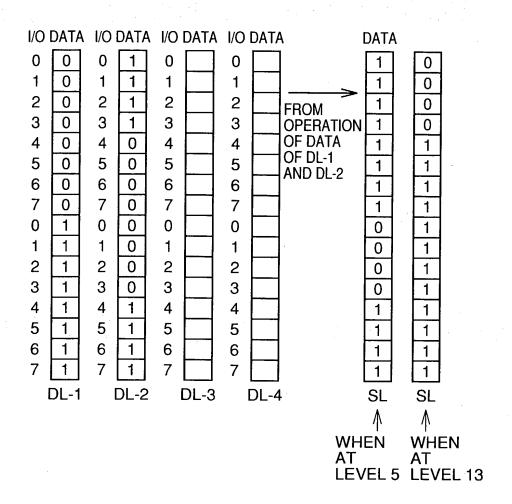
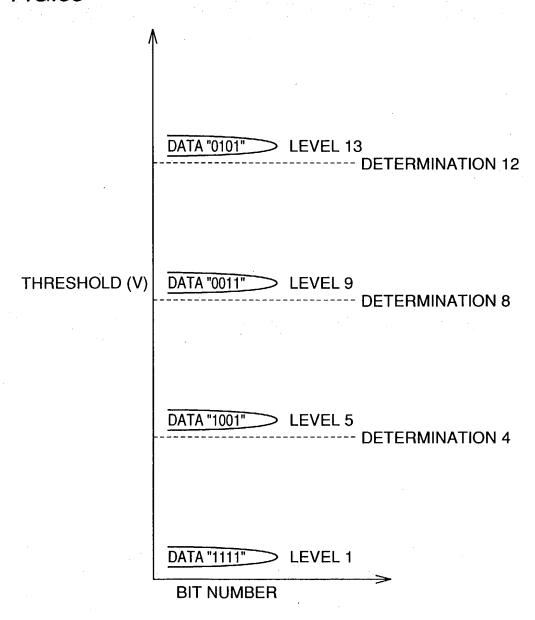




FIG.85





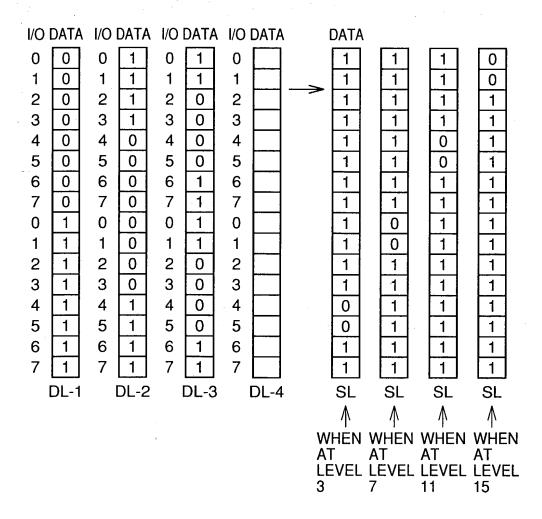




FIG.87

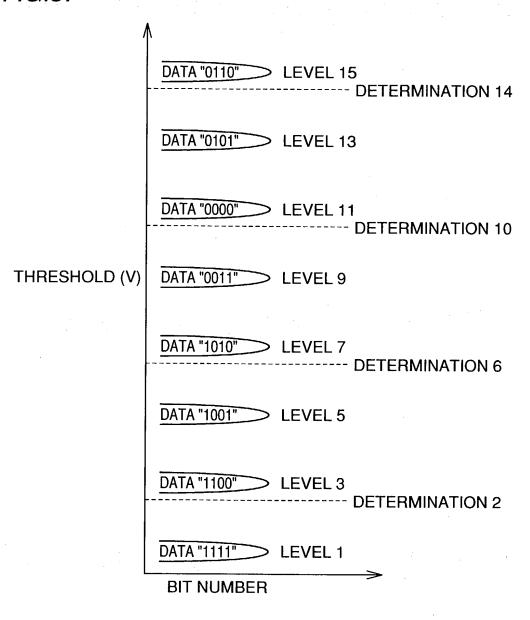




FIG.88

I/O DATA	I/O	DATA	I/O	DATA		DATA
I/O DATA 0	1/O 0 1 2 3 4 5 6 7 0 1 2 3 4 5	1 1 1 1 0 0 0 0 0 0	I/O 0 1 2 3 4 5 6 7 0 1 2 3 4 5	DATA	FROM DL-1	DATA 0 0 0 0 0 0 1 1 1 1 1 1
5	5 6					-
7	7	1	6 7			1
DL-1		DL-2		DL-3		SL
	H	NPU ¹	Γ		•	



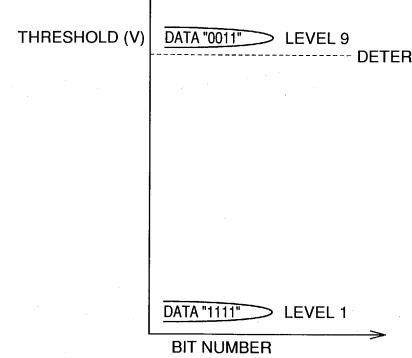




FIG.90

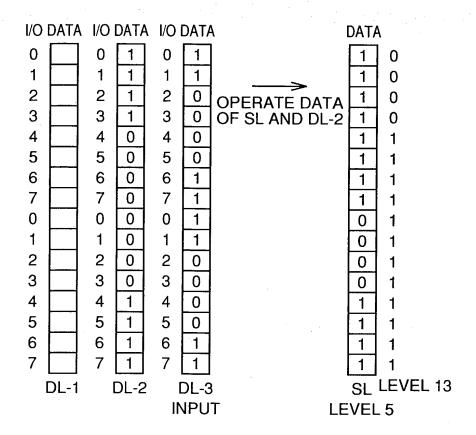
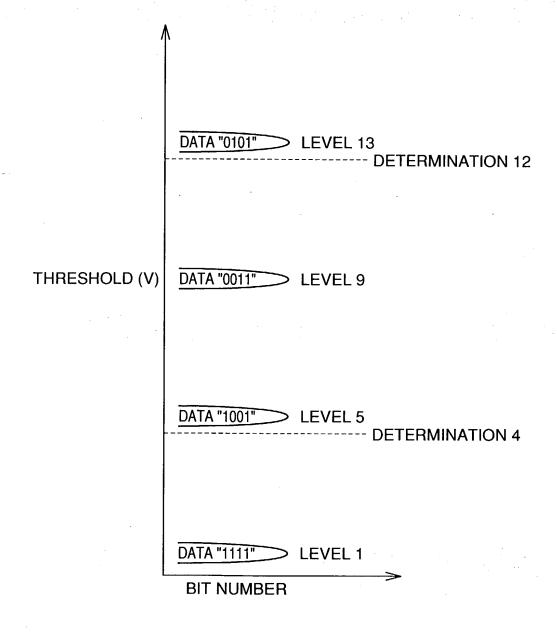




FIG.91





I/O I	DATA	1/0	DATA	1/0	DATA	A D)ATA
0	1	0	1	0	1		0
1	1	1	0	1	1		0
2	1	2	0	2	0	INVERTED DATA	0
3	1	3	1	3	0	OF SL TO DL-1	0
4	1	4	1	4	0		0
5	1	5	0	5	0		0
6	1	6	0	6	1		0
7	1	7	1	7	1		0
0	0	0	1	0	1	, ,	1
1	0	1	0	1	1	Ī	1
2	0	2	0	2	0		1
3	0	3	[1]	3	0		1
4	0	4	1	4	0		1
5	0	5	0	5	0		1
6	0	6	0	6	1		1
7	0	7	1	7	1		1
[DL-1	I	DL-2	! 1	DL-3	3	SL
		11	NPU	T		READ A	
						DETERI	8 MINATION 8



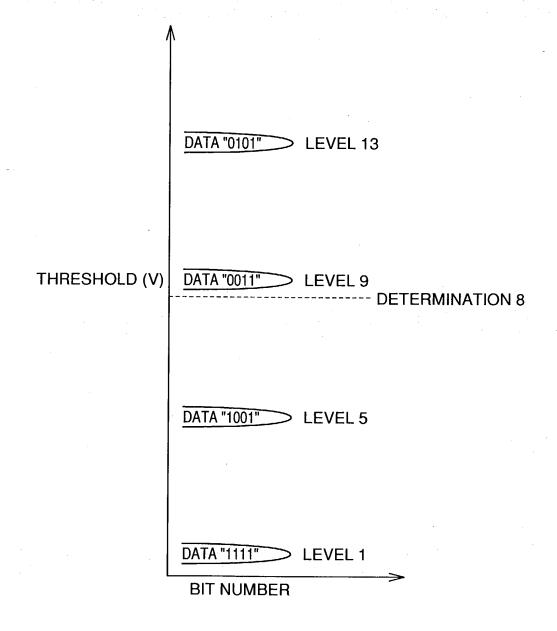
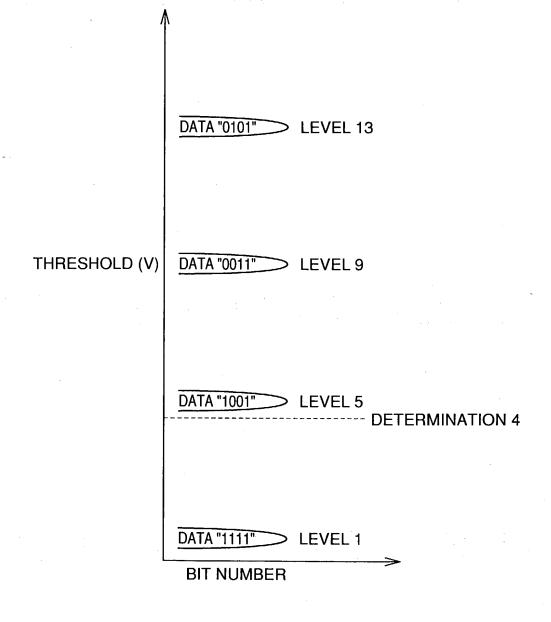




	FIG.94		
	I/O DATA I/O DATA I	O DATA	DATA
		0 1	0
	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	1 1 2 0 0 DATA OF SI	0 0
		2 0 OR DATA OF SL 3 0 AND DL-1 AND	0
		4 0 STORE RESULT	0
		5 0 IN DL-1 6 1	0
Teat		7 1	0
		0 1	0
	1 0 1 0 2 0	1 1 2 0	0
		3 0	0 0
	4 1 4 1	4 0	1
		5 <u>0</u> 6 1	1 2
	<u> </u>	6 <u>1</u> 7 1	
	DL-1 DL-2	DL-3	SL
	INPUT	READ DETER	AT RMINATION 4



FIG.95



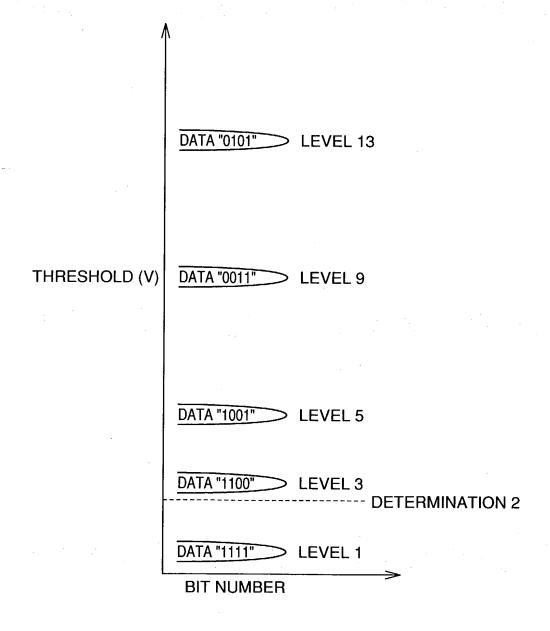


 $\mathcal{O}_{\mathcal{A}} = \{ (1, 1) \mid \mathcal{O}_{\mathcal{A}} = \{ (1,$

F	IG.96			
	I/O DATA I/O DATA	I/O DATA	DATA	
	0 1 0 1	0 1	1	
	1 1 0	1 1	← 1	
	2 1 2 0 3 1	2 0 OPE	RATE DATA	
	3 1 3 1 4 1	3 0 OF S	SL AND DL-3 1	
	5 1 5 0	5 0		
	$6 \mid 1 \mid 6 \mid 0$	6 1	1	
g Williams	7 1 7 1	7 1	11	
	0 0 0 1	0 1	1	
	1 0 1 0	1 1	1	
	2 0 2 0	2 0	1	
	3 0 3 1	3 0	1	
	4 1 4 1	4 0	0	
	5 1 5 0	5 0	0	
	6 1 6 0 7 1 7 1	6 <u>1</u> 7 <u>1</u>	1	
	DL-1 DL-2	DL-3	SL	
	INPU ⁻	Γ	WRITE LEVEL 3	



FIG.97





1/0 1	DATA	I/O	DATA	I/O	DATA		DATA
0	1	0	1	0	1		1
1	1	1	0	1	1	_ · ~	1
2	1	2	0	2	0	OPERATE	DATA 1
3	1	3	1	3	0	OF DL-1 AN	
4	1	4	1	4	0	DL-3	1
5	1	5	0	5	0	TO SL	1
6	1	6	0	6	1		1
7	1	7	1	7	1		1
0	0	0	1	0	1		0
1	0	1	0	1	1		0
2	0	2	0	2	0		1
3	0	3	1	3	0		1
4	1	4	1	4	0		1
5	1	5	0	5	0		1
6	1	6	0	6	1		1
7	1	7	1	7	1		1
[DL-1	I	DL-2		DL-3		SL
		11	NPUT	•			WRITE LEVEL 7



DATA "0101" > LEVEL 13 THRESHOLD (V) DATA "0011" LEVEL 9 -- DETERMINATION 6 DATA "1001" LEVEL 5 DATA "1100" LEVEL 3 DATA "1111" > LEVEL 1 **BIT NUMBER**



I/O D	ATA	I/O	DATA	1/0	DATA		DATA
0 [0	0	1	0	1		0
1	0	1	0	1	1	← →	0
2 [0	2	0	2	0	TRANSFER	0
3 [0	3	1	3	0	FROM SL	0
4	0	4	1	4	0	TO DL-1	0
5	0	5	0	5	0		0
6	0	6	0	6	1		0
7 [0	7	1	7	1		0
0	1	0	1	0	1		1
1	1	1	0	1	1		1
2	1	2	0	2	0		1
3	1	3	1	3	0		1
4	1	4	1	4	0		1
5	1	5	0	5	0		1
6	1	6	0	6	1		1
7	1	7	1	7	1		1
D	L-1	i	DL-2	ı	DL-3		SL
		11	NPU	Γ		REA	D AT
						DET	ERMINATION 8



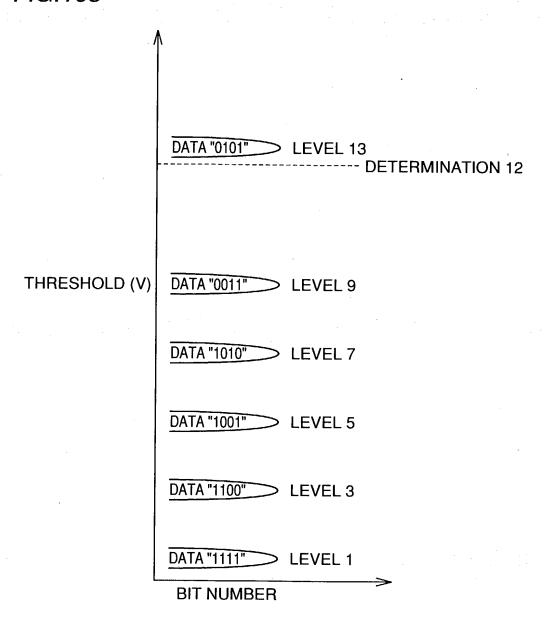
DATA "0101" THRESHOLD (V) DATA "1001" LEVEL 7 DATA "1001" > LEVEL 5 DATA "1100" > LEVEL 3 BIT NUMBER



	FIG.102		
	I/O DATA I/O DATA I/O DATA	DATA	•
	0 1 0 1 0 1	0	
	1 1 1 0 1 1	0	
		OR INVERTED 0	
		DATA OF SL 0 AND DATA OF 1	
		DL-1 AND	
•		STORE RESULT 1	
in the	7 0 7 1 7 1	1	
	0 1 0 1 0 1	1	
		1	
•	2 1 2 0 2 0 3 1 3 0	1	
	4 1 4 1 4 0	1	
	5 1 5 0 5 0	1	
	6 1 6 0 6 1	1	
	7 1 7 1 7 1	1	
	DL-1 DL-2 DL-3	SL	
	INPUT	READ AT DETERMINATION 12	



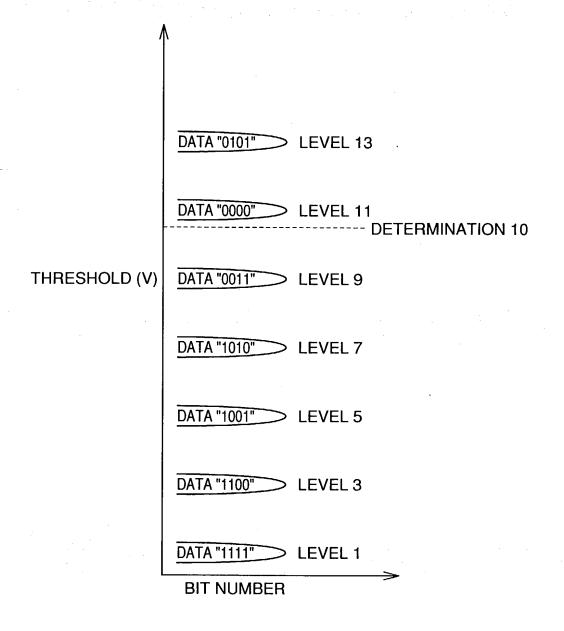
FIG.103





I/O	DATA	I/O	DATA	I/O	DATA	A DATA
0	1	0	1	0	1	1
1	1	1	0	1	1	
2	1	2	0	2	0	OPERATE DATA
3	1	3	1	3	0	OF DL-1 AND 1
4	0	4	1	4	0	DL-3
5	0	5	0	5	0	TO SL 0
6	0	6	0	6	1	1
7	0	7	1	7	1	1
0	1	0	1	0	1	1
1	1	1	0	1	1	1
2	1	2	0	2	0	1
3	1	3	1	3	0	· [1]
4	1	4	1	4	0	1
5	1	5	0	5	0	1
6	1	6	0	6	1	1
7	1	7	1	7	1	1
[DL-1		DL-2	I	DL-3	SL SL
		lî.	NPU1			WRITE LEVEL 11







I/O	DATA	A I/O	DATA	1/01	DATA	A DATA
0	1	0	1	0	1	
1	1	1	0	1	1	0
2	1	2	0	2	0	OPERATE DATA
3	1	3	1	3	0	OF DL-1 AND 0
4	0	4	1	4	0	DL-3
5	0	5	0	5	0	TO SL 1
6	0	6	0	6 ·	1	1
7	0	7	1	7	1	1
0	0	0	1	0	1	1
1	0	1	0	1	1	. 1
2	0	2	0	2	0	1
3	0	3	1	3	0	1
4	1	4	1	4	0	1
. 5	1	-5	0	5	0	1
6	1	6	0	6	1	1
7	1	7	1	7	1	1
I	DL-1	[DL-2	. [DL-3	SL SL
		IN	NPU.	Τ		READ AT
						DETERMINATION 12



FIG.107

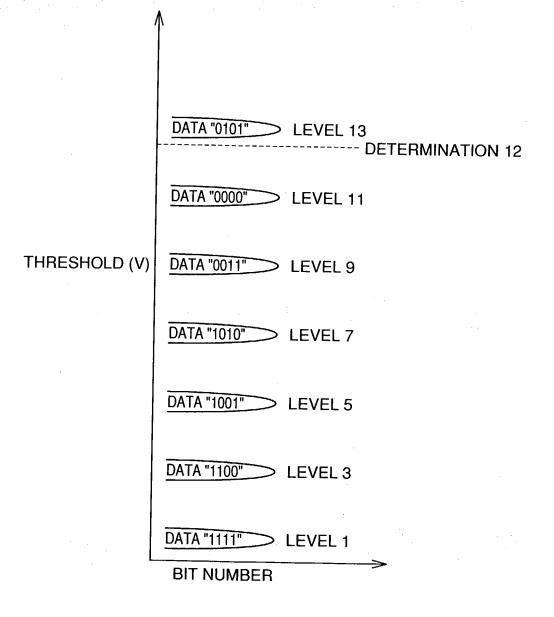
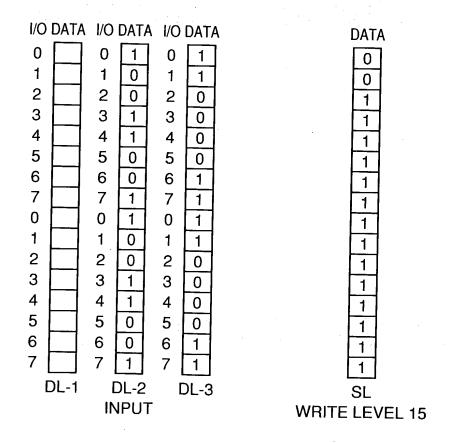
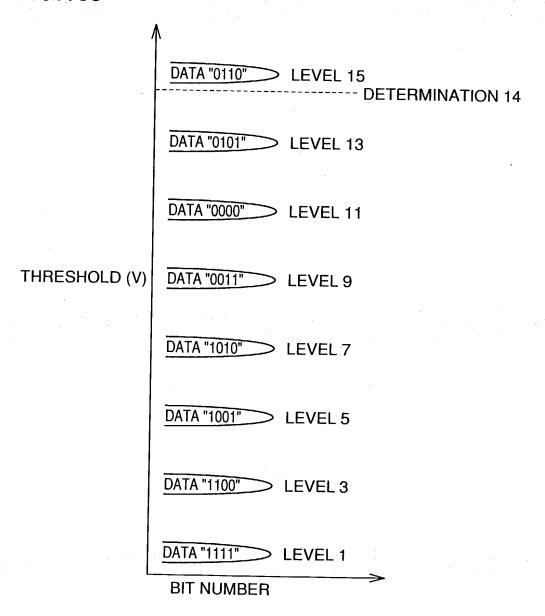




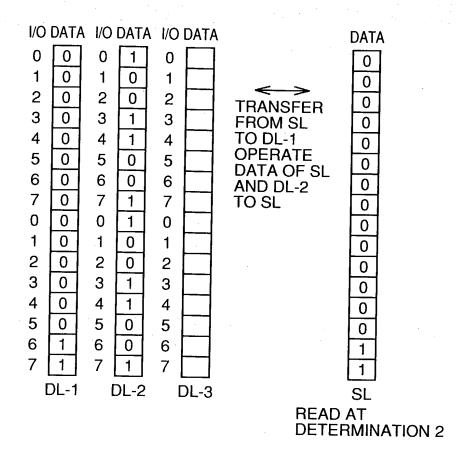
FIG.108



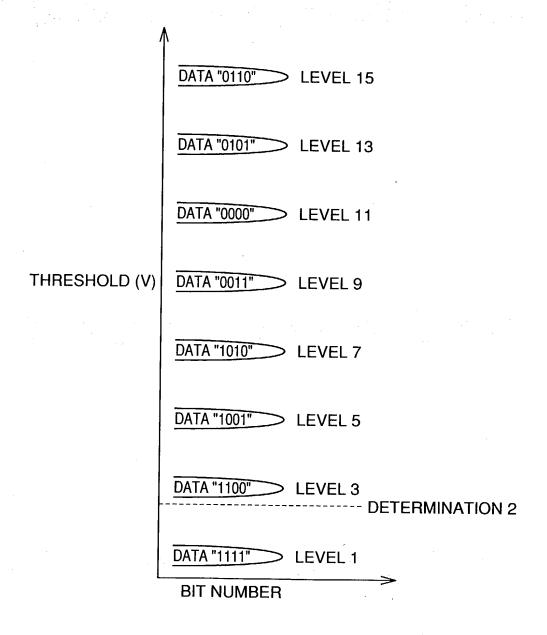














ÍΩ	DATA	1/0	חאדא	I/O DATA	D.4.T.4
					DATA
0	0	0	1	0	[1]
1	0	1	0	1	1
2	0	2	0	2	11
3	0	3	1	3	1
4	0	4	1	4	1
5	0	5	0	5	1
6	0	6	0	6	1
7	0	7	1	7	1
0	.0	0	1		1
1	0	1	0	1	1
2	0	2	0	2	1
3	0	3	1	$\frac{1}{3}$	1
4	0	4	计	4	├
5	 	5	0	5	1
6	1	1			1
	-	6	0	6	0
7 [7 [7	1
)L-1)L-2	DL-3	SL
					WRITE LEVEL 2



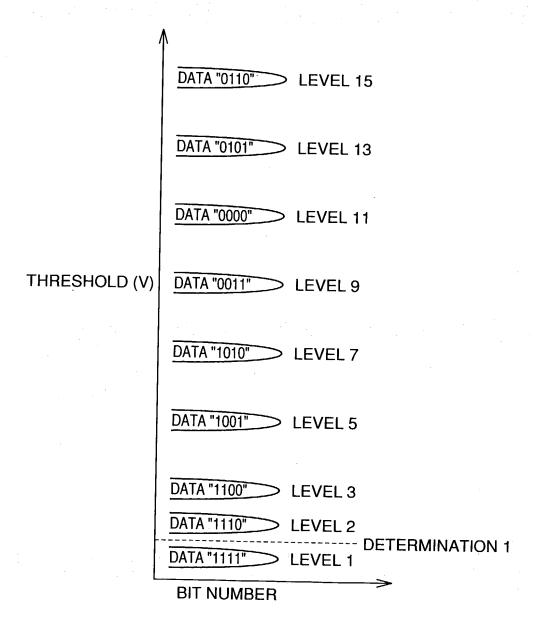
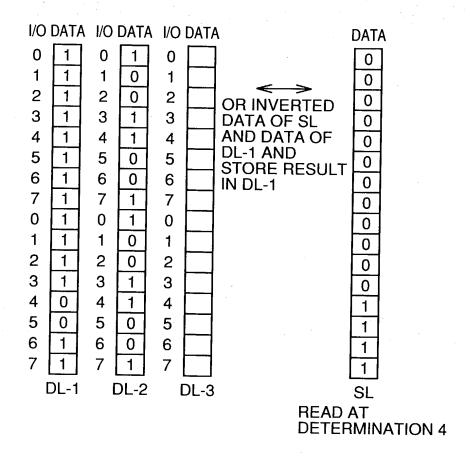




FIG.114





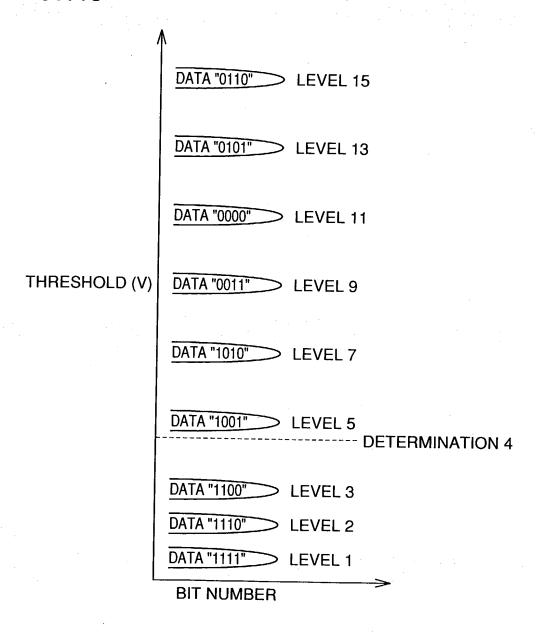
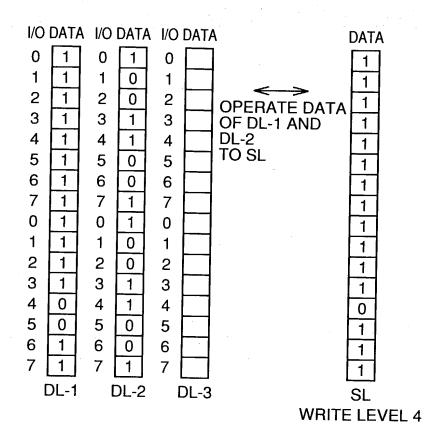




FIG.116





	↑
	DATA "0110" LEVEL 15
	DATA "0101" LEVEL 13
	DATA "0000" LEVEL 11
THRESHOLD (V)	DATA "0011" LEVEL 9
	DATA "1010" LEVEL 7
	DATA "1001" LEVEL 5
	DATA "1001" LEVEL 4
	DATA "1100" LEVEL 3
	DATA "1110" LEVEL 2
	DATA "1111" LEVEL 1
L	BIT NUMBER



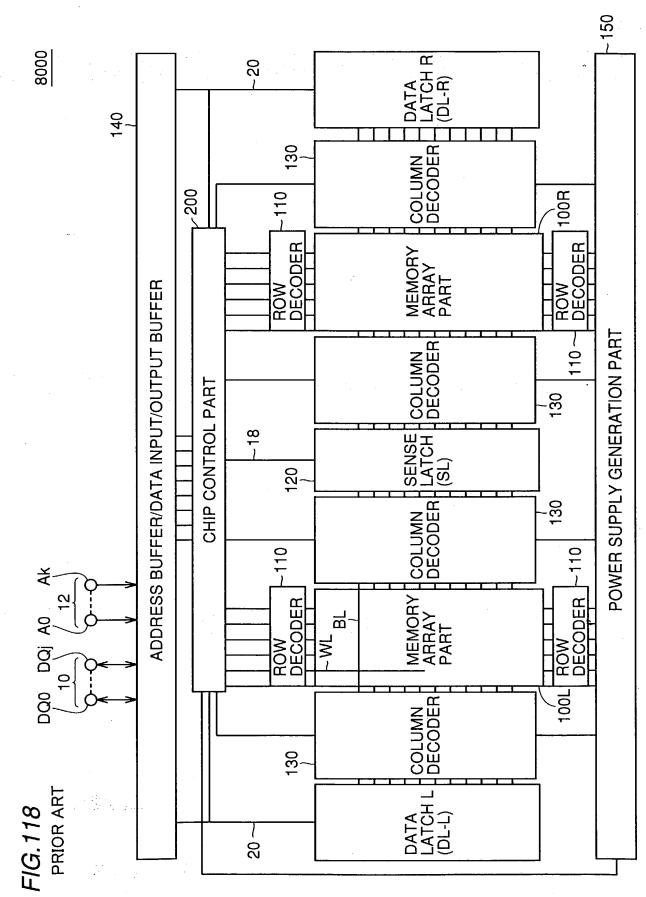




FIG.119 PRIOR ART

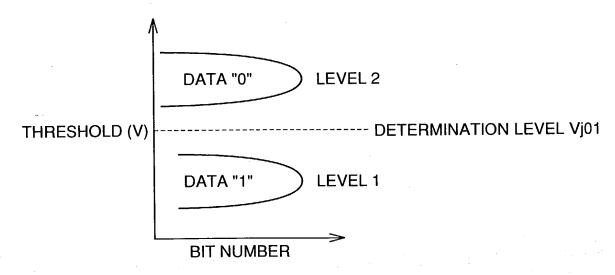


FIG. 120 PRIOR ART

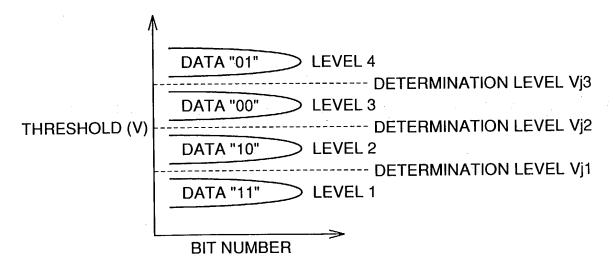




FIG. 121 PRIOR ART

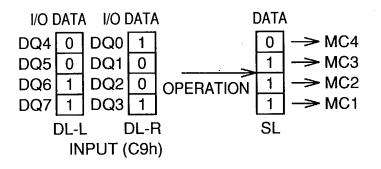


FIG. 122 PRIOR ART

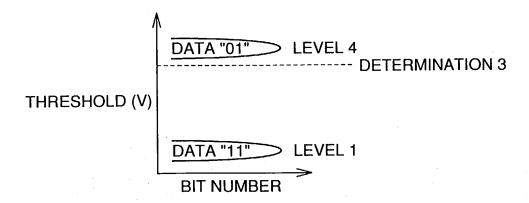




FIG. 123 PRIOR ART

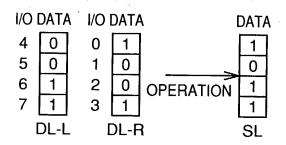


FIG. 124 PRIOR ART

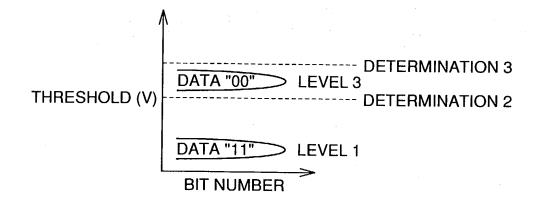




FIG. 125 PRIOR ART

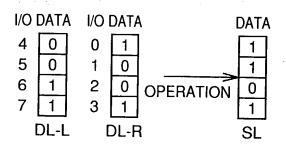


FIG.126 PRIOR ART

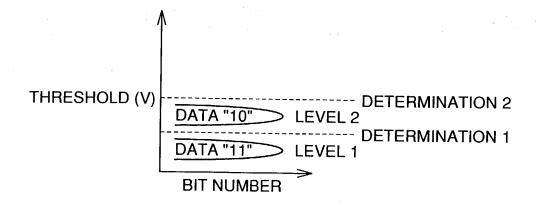




FIG. 127 PRIOR ART

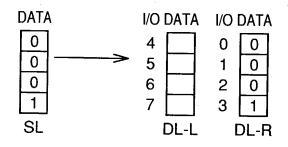


FIG. 128 PRIOR ART

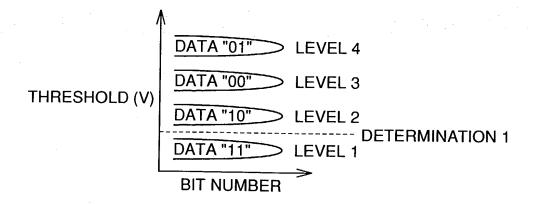




FIG. 129 PRIOR ART

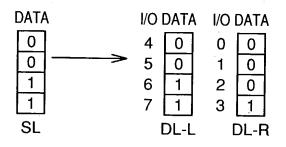


FIG.130 PRIOR ART

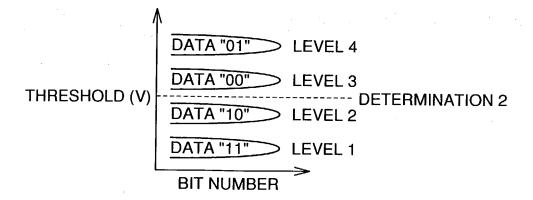




FIG.131 PRIOR ART

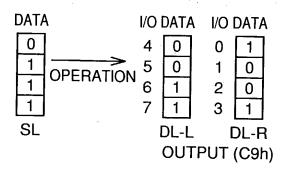


FIG. 132 PRIOR ART

